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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/852,847	05/11/2001	Shinji Ohuchi	OKI.234	5682

7590 01/02/2003

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EXAMINER

LEWIS, MONICA

ART UNIT	PAPER NUMBER
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2822

DATE MAILED: 01/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/852,847

Applicant(s)

OHUCHI ET AL.

Examiner

Monica Lewis

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 October 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 18-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 18-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☒ The proposed drawing correction filed on 15 October 2002 is: a) ☒ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

1. This action is in response to the amendment filed October 15, 2002.

Response to Arguments

2. Applicant's arguments with respect to claims 18-27 have been considered but are moot in view of the new ground(s) of rejection.

Specification

3. The disclosure is objected to because "The Brief Description of the Drawings" does not describe the following figures: a) Figures 16a-16c.

Appropriate correction is required.

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 18-22 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art Drawings in view of Ouchi et al. (Japan Patent No. 10-261753).

In regards to claim 18, Applicant's Prior Art Drawings discloses the following:

a) a semiconductor element (601) having a circuit forming surface (See Figure 21);

Art Unit: 2822

b) a wiring (604) disposed on said circuit forming surface and on a side surface (See Figure 21 and 22);

c) a sealed bump electrode (602) connected to said wiring (See Figure 21 and);

d) sealed bump electrode having an exposed surface (See Figure 21); and

e) a ball electrode (603) disposed on said exposed surface of said bump electrode (See Figure 21).

In regards to claim 18, Applicant's Prior Art Drawings fail to disclose the following:

a) sealed confronting surface of said circuit forming surface.

However, Ohuchi et al. ("Ohuchi) discloses a sealed circuit forming surface (See Figure 3b and Abstract). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include a sealed circuit forming surface as disclosed in Ohuchi because it aids in protecting the device from extremities.

In regards to claim 19, Applicant's Prior Art Drawings discloses the following:

a) a plurality of electrodes on said circuit forming surface (See Figure 21).

In regards to claim 20, Applicant's Prior Art Drawings fail to disclose the following:

a) wiring on a side surface has an end that is sealed (See Figure 21 and 22).

In regards to claim 21, Applicant's Prior Art Drawings discloses the following:

a) sealed bump electrode is resin sealed (See Specification Page 2 Lines 1 and 2).

In regards to claim 21, Applicant's Prior Art Drawings fail to disclose the following:

a) sealed confronting surface is resin sealed.

However, Ohuchi discloses a sealed circuit forming surface (See Figure 3b and Abstract).

It would have been obvious to one having ordinary skill in the art at the time the invention was

Art Unit: 2822

made to modify the semiconductor device of Applicant's Prior Art Drawings to include a sealed circuit forming surface as disclosed in Ohuchi because it aids in protecting the device from extremities.

In regards to claim 22, Applicant's Prior Art Drawings fail to disclose the following:

a) sealed confronting surface is entirely sealed.

However, Ohuchi discloses a sealed circuit forming surface (See Figure 3b and Abstract). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include a sealed circuit forming surface as disclosed in Ohuchi because it aids in protecting the device from extremities.

In regards to claim 27, Applicant's Prior Art Drawings fail to disclose the following:

a) a part of said ball electrode is disposed on said wiring disposed on said side surface of said semiconductor element.

However, Ohuchi discloses a ball electrode on wire (See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include a ball electrode disposed on wire as disclosed in Ohuchi because it aids in providing communication among the various components.

Art Unit: 2822

7. Claims 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art Drawings in view of Ouchi et al. (Japan Patent No. 10-261753) and Hatano et al. (U.S. Patent No. 6,104,088).

In regards to claim 23, Applicant's Prior Art Drawings fail to disclose the following:

a) a semiconductor device mounted on a second semiconductor device.

However, Hatano discloses two semiconductor devices mounted on each other (See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include two semiconductor devices mounted on each other as disclosed in Hatano because it aids in increasing the memory density.

In regards to claim 24, Applicant's Prior Art Drawings fail to disclose the following:

a) another semiconductor device has electrodes that are connected to said wiring of the semiconductor device.

However, Hatano discloses two semiconductor devices mounted on each other where the second device has electrodes (See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include two semiconductor devices mounted on each other via electrodes as disclosed in Hatano because it aids in increasing the memory density.

In regards to claim 25, Applicant's Prior Art Drawings fail to disclose the following:

a) semiconductor device is mounted on another semiconductor device with said confronting surface as a contacting has electrodes that are connected to said wiring of the semiconductor device and to at least one of said plurality of electrodes.

However, Hatano discloses two semiconductor devices mounted on each other where the second device has electrodes (See Figure 1). It would have been obvious to one having ordinary

Art Unit: 2822

skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include two semiconductor devices mounted on each other via electrodes as disclosed in Hatano because it aids in increasing the memory density.

In regards to claim 26, Applicant's Prior Art Drawings fail to disclose the following:

a) another semiconductor device is disposed over a plurality of other semiconductor devices (See Figure 1).

However, Hatano discloses a semiconductor device disposed over other devices (See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include a semiconductor device disposed over other devices as disclosed in Hatano because it aids in increasing the memory density.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Art Unit: 2822

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML

December 27, 2002


AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
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